Video Module Interface (VMI) for ICs

Author: Keith Jack

Introduction

VMI was developed in cooperation with several multimedia IC companies in order to standardize the video interfaces between devices such as MPEG decoders, NTSC/PAL decoders, and GUI accelerators. It is primarily based on the output interface and timing of the Philip's SAA7111 NTSC/PAL decoder.

Video Data Format

An 8-bit 4:2:2 YCbCr interface is normally used, similar to that used by the BT.656 parallel interface. However, the EAV and SAV sequences that BT.656 uses are not present.

The 4:2:2 YCbCr data is multiplexed into an 8-bit stream: $Cb_0Y_0Cr_0Y_1Cb_2Y_2Cr_2$, etc. Figures 1 and 2 illustrate the format for 525/60 and 625/50 video systems, respectively, using 8-bit YCbCr data.

The stream of active data words always begins with a Cb sample. In the multiplexed sequence, the co-sited samples (those that correspond to the same point on the picture) are grouped as Cb, Y, Cr.

VMI does not define a specific pixel clock rate. However, most rectangular pixel applications sample each line of video at 13.5MHz, generating 720 active samples of 24-bit 4:4:4 YCbCr data, as shown in Figures 3 and 4. This is converted to 16-bit 4:2:2 YCbCr data, resulting in 720 active samples of Y per line, and 360 active samples each of Cb and Cr per line. The Y data and the CbCr data are multiplexed, and the 13.5MHz sample clock rate is increased by two to 27MHz.

VMI also does not define any horizontal or vertical blanking intervals, using instead a programmable blanking signal (VACTIVE). For most rectangular pixel applications, the vertical blanking intervals will be as shown in Figures 5 and 6. Note that active resolutions other than 720 x 486 and 720 x 576 may be supported (effectively cropping the image) by adjusting the timing of VACTIVE.

Square Pixel Variation

A variation using square pixels may also be used. Instead of a 27MHz clock, a 24.54MHz clock is used for 525/60 video systems (640 x 480 active resolution), and a 29.5MHz clock is used for 625/50 video systems (768 x 576 active resolution).

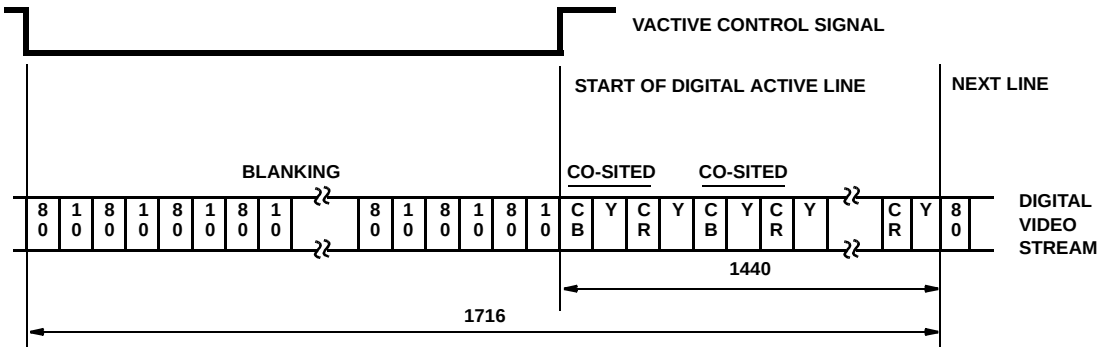


FIGURE 1. TYPICAL VMI 8-BIT DATA FORMAT FOR RECTANGULAR PIXEL 525/60 VIDEO SYSTEMS

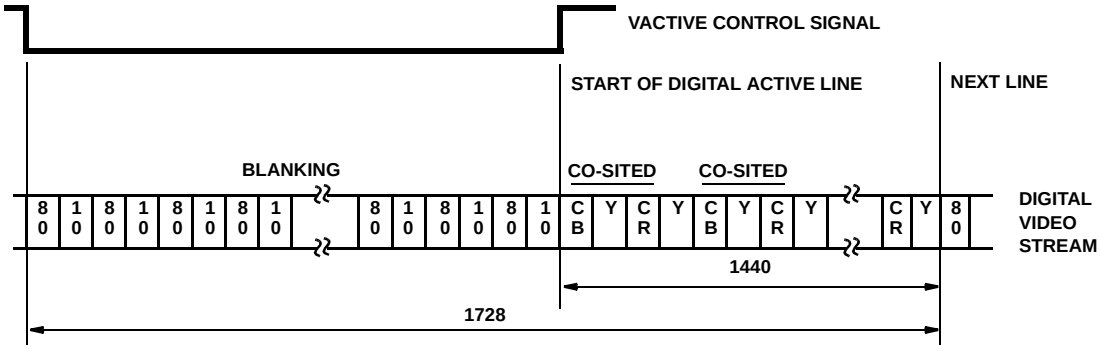


FIGURE 2. TYPICAL VMI 8-BIT DATA FORMAT FOR RECTANGULAR PIXEL 625/50 VIDEO SYSTEMS

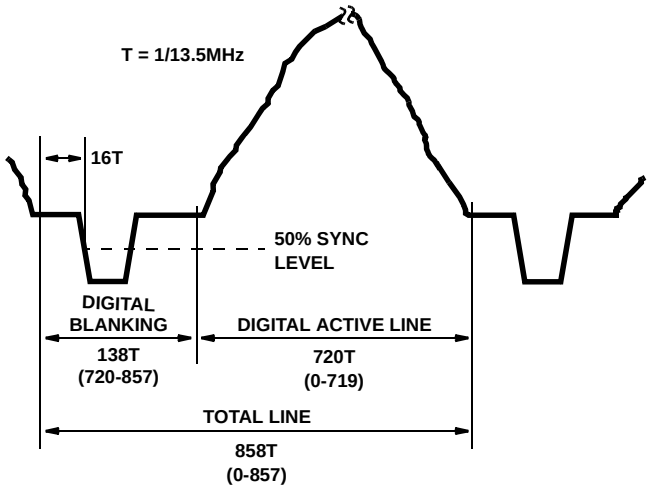


FIGURE 3. TYPICAL VMI HORIZONTAL TIMING RELATIONSHIP FOR RECTANGULAR PIXEL 525/60 VIDEO SYSTEMS

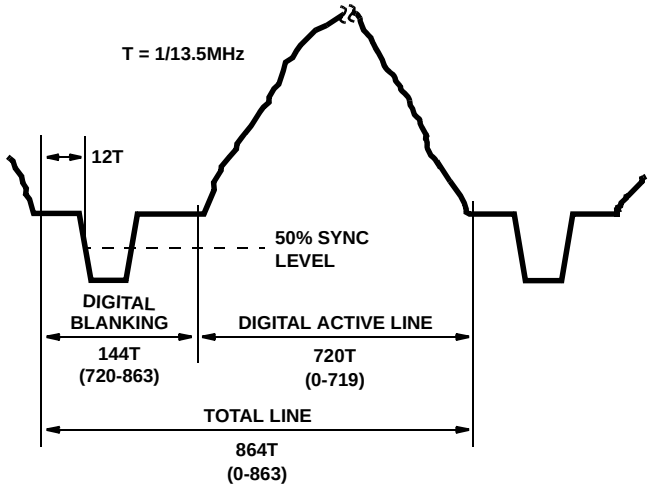


FIGURE 4. TYPICAL VMI HORIZONTAL TIMING RELATIONSHIP FOR RECTANGULAR PIXEL 625/50 VIDEO SYSTEMS

Figures 7 and 8 illustrate the data format, Figures 9 and 10 illustrate the typical horizontal timing relationships, and Figures 11 and 12 show the typical vertical blanking intervals.

16-Bit YCbCr Variation

Although not a part of the VMI specification, a variation using 16-bit 4:2:2 YCbCr data is common, as shown in Figures 13 and 14. In this instance, the PIXCLK signal is one-half the normal clock rate: 13.5MHz, 12.27MHz (square pixel 525/60 video systems) or 14.75MHz (square pixel 625/50 video systems).

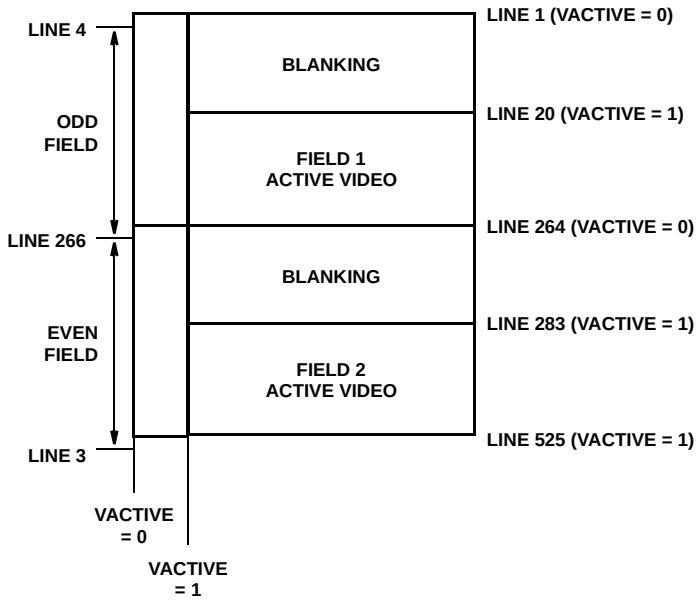
Video Timing Signals

In addition to the pixel data, there are four video timing signals, consisting of VREF, HREF, VACTIVE, and PIXCLK. To support video sources that do not generate a line-locked clock, a Data Valid signal (DVALID) is also commonly used.

VREF and HREF can be considered to be VSYNC and HSYNC signals, respectively. If HREF is high during the falling edge of VREF, the field is odd. If HREF is low during the falling edge of VREF, the field is even. Thus, even/odd field detection is done using the trailing edge of VREF, rather than the leading edge, as with most video systems. Figures 15 and 16 illustrate the HREF and VREF timing for 525/60 and 65/50 video systems, respectively.

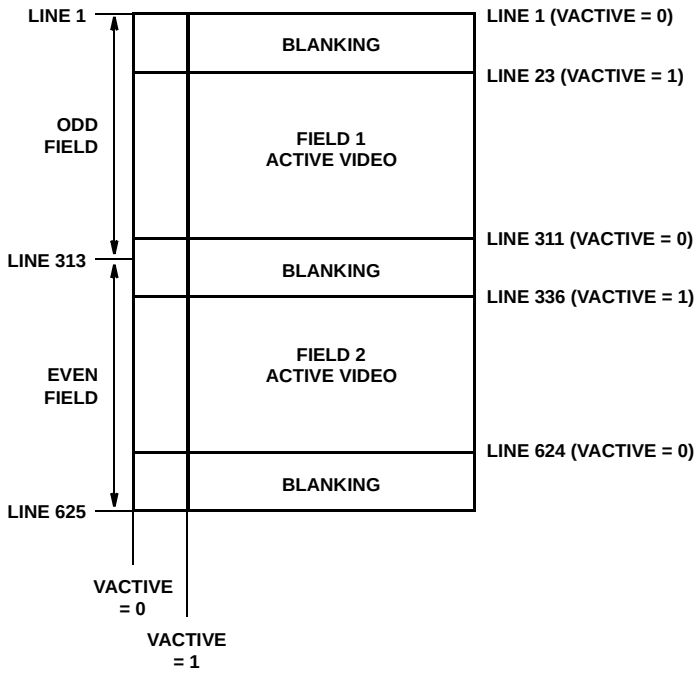
VACTIVE can be considered a blanking signal, and indicates that valid pixel data is being transmitted across the YCbCr bus. If a DVALID signal is also used, valid pixel data is present when both VACTIVE and DVALID are asserted.

For 8-bit YCbCr interfaces, PIXCLK is a 2x pixel clock. For 16-bit YCbCr interfaces, PIXCLK is a 1x pixel clock.



LINE NUMBER	FIELD	VACTIVE
1-3	1	0
4-19	0	0
21-263	0	1
264-265	0	0
266-282	1	0
283-525	1	1

FIGURE 5. TYPICAL VMI VERTICAL BLANKING INTERVALS FOR RECTANGULAR PIXEL 525/60 VIDEO SYSTEMS



LINE NUMBER	FIELD	VACTIVE
1-22	0	0
23-310	0	1
311-312	0	0
313-335	1	0
336-623	1	1
624-625	1	0

FIGURE 6. TYPICAL VMI VERTICAL BLANKING INTERVALS FOR RECTANGULAR PIXEL 625/50 VIDEO SYSTEMS

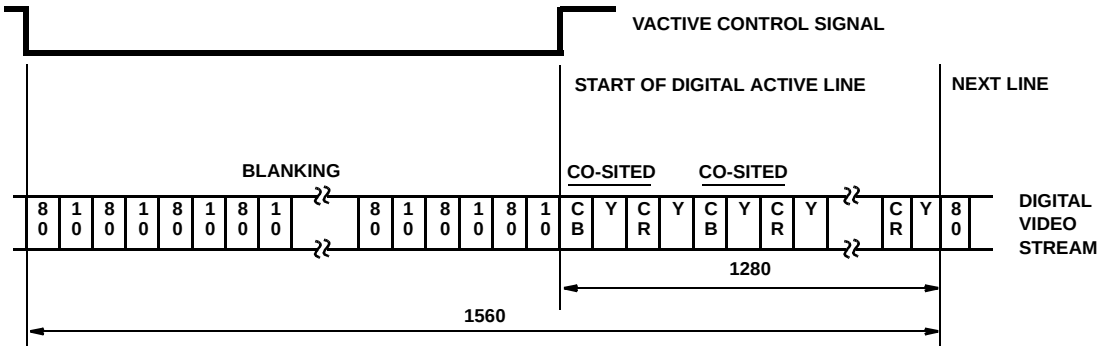


FIGURE 7. TYPICAL VMI DATA FORMAT FOR SQUARE PIXEL 525/60 VIDEO SYSTEMS

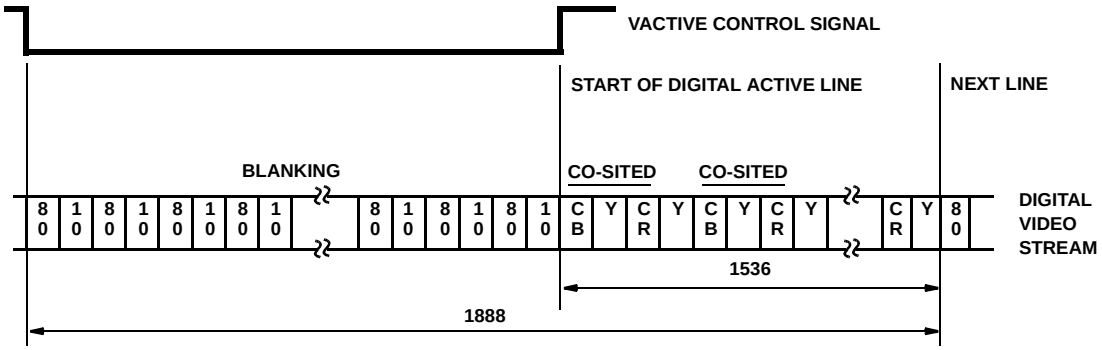


FIGURE 8. TYPICAL VMI DATA FORMAT FOR SQUARE PIXEL 625/50 VIDEO SYSTEMS

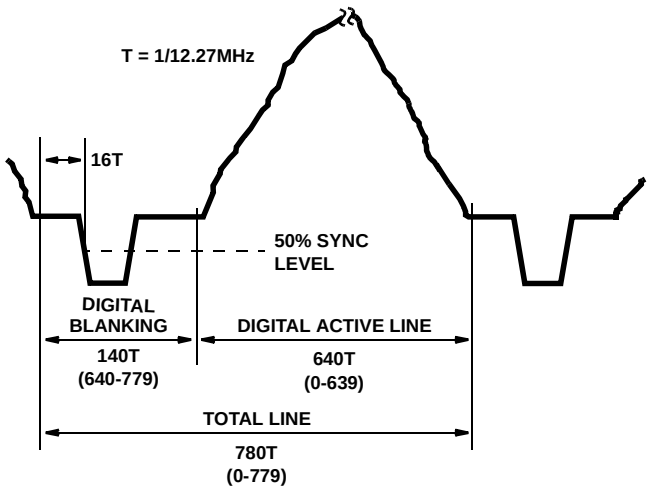


FIGURE 9. TYPICAL VMI HORIZONTAL TIMING RELATIONSHIP FOR SQUARE PIXEL 525/60 VIDEO SYSTEMS

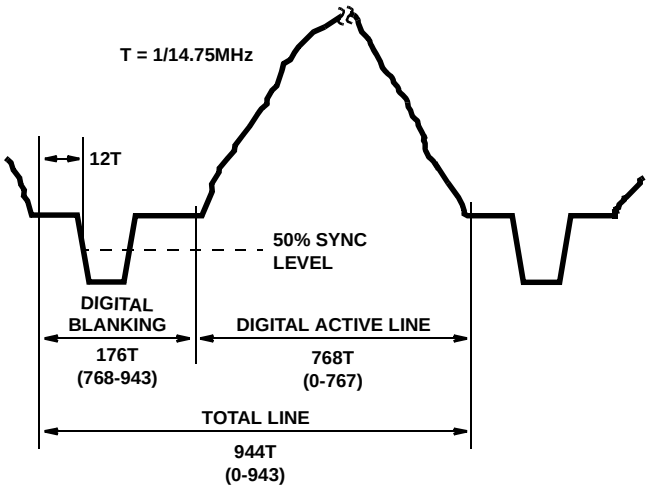
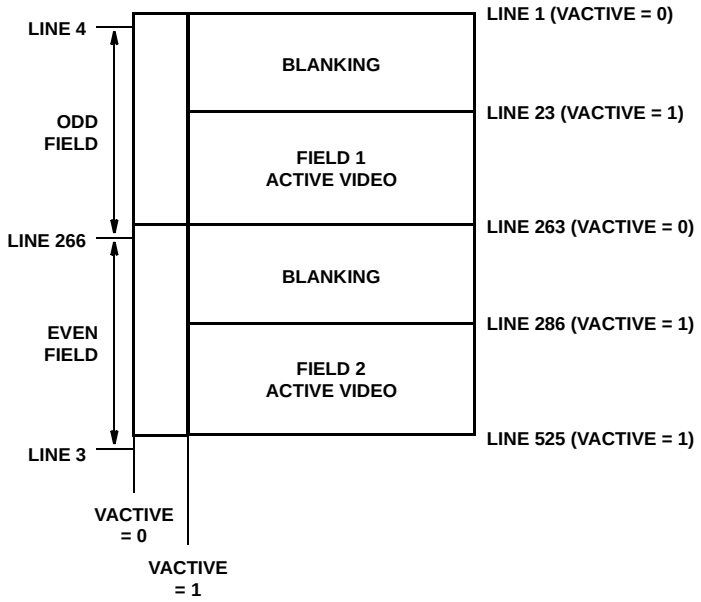
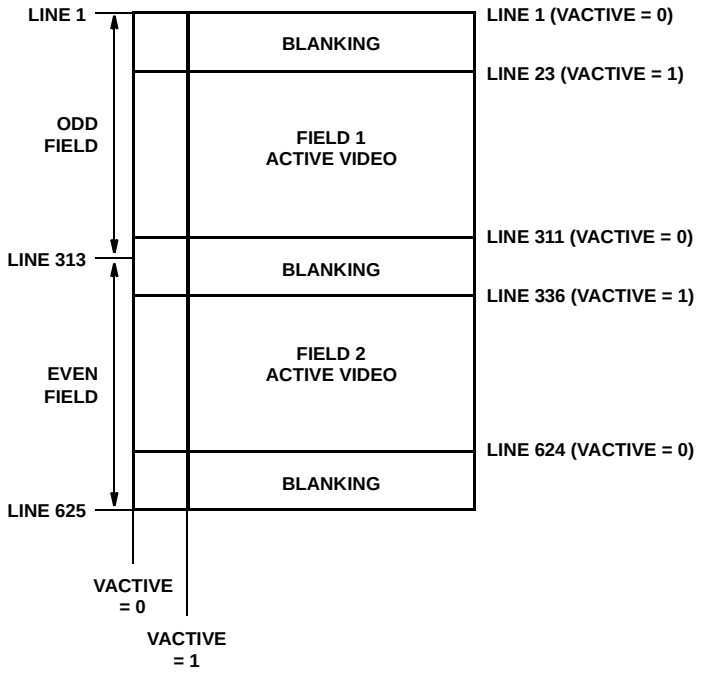


FIGURE 10. TYPICAL VMI HORIZONTAL TIMING RELATIONSHIP FOR SQUARE PIXEL 625/50 VIDEO SYSTEMS



LINE NUMBER	FIELD	VACTIVE
1-3	1	0
4-22	0	0
23-262	0	1
263-265	0	0
266-285	1	0
286-525	1	1

FIGURE 11. TYPICAL VMI VERTICAL BLANKING INTERVALS FOR SQUARE PIXEL 525/60 VIDEO SYSTEMS



LINE NUMBER	FIELD	VACTIVE
1-22	0	0
23-310	0	1
311-312	0	0
313-335	1	0
336-623	1	1
624-625	1	0

FIGURE 12. TYPICAL VMI VERTICAL BLANKING INTERVALS FOR SQUARE PIXEL 625/50 VIDEO SYSTEMS

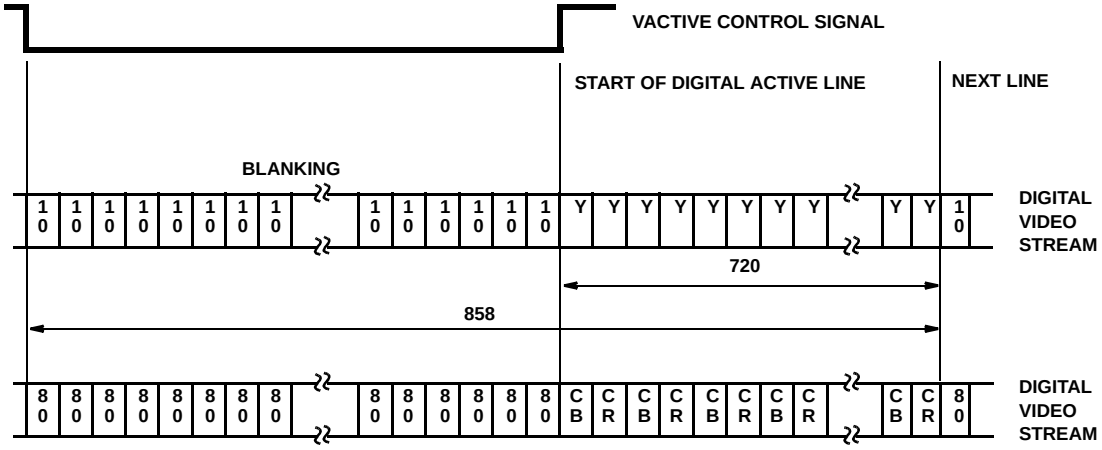


FIGURE 13. TYPICAL VMI 16-BIT DATA FORMAT FOR RECTANGULAR PIXEL 525/60 VIDEO SYSTEMS

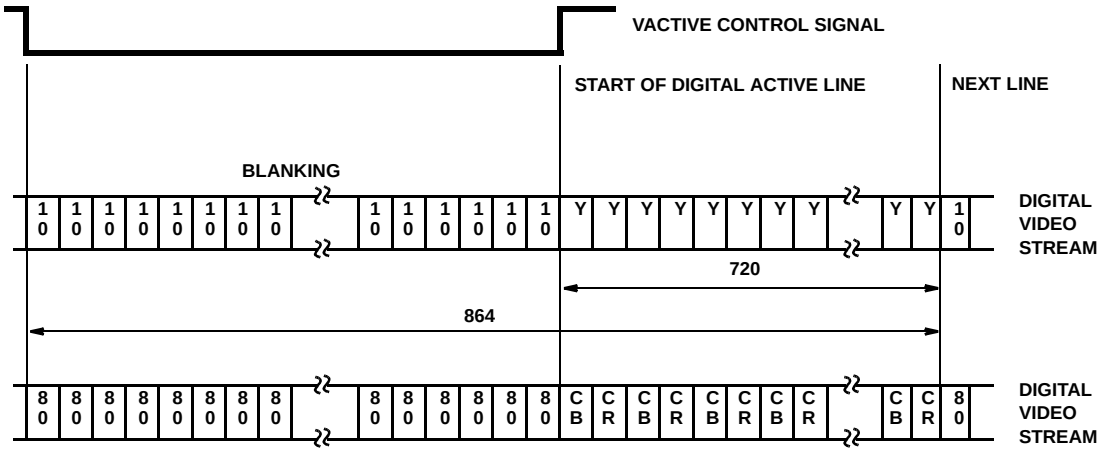


FIGURE 14. TYPICAL VMI 16-BIT DATA FORMAT FOR RECTANGULAR PIXEL 625/50 VIDEO SYSTEMS

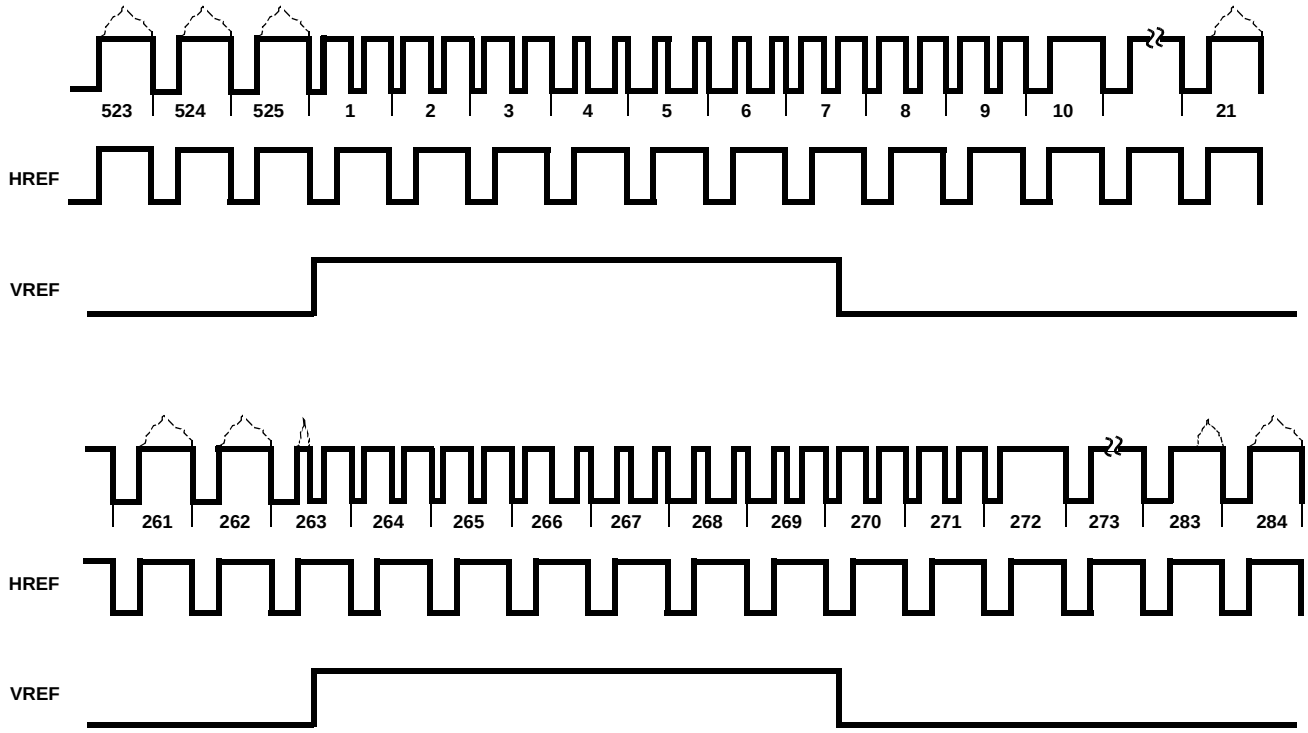


FIGURE 15. HREF AND VREF TIMING FOR 525/60 VIDEO SYSTEMS

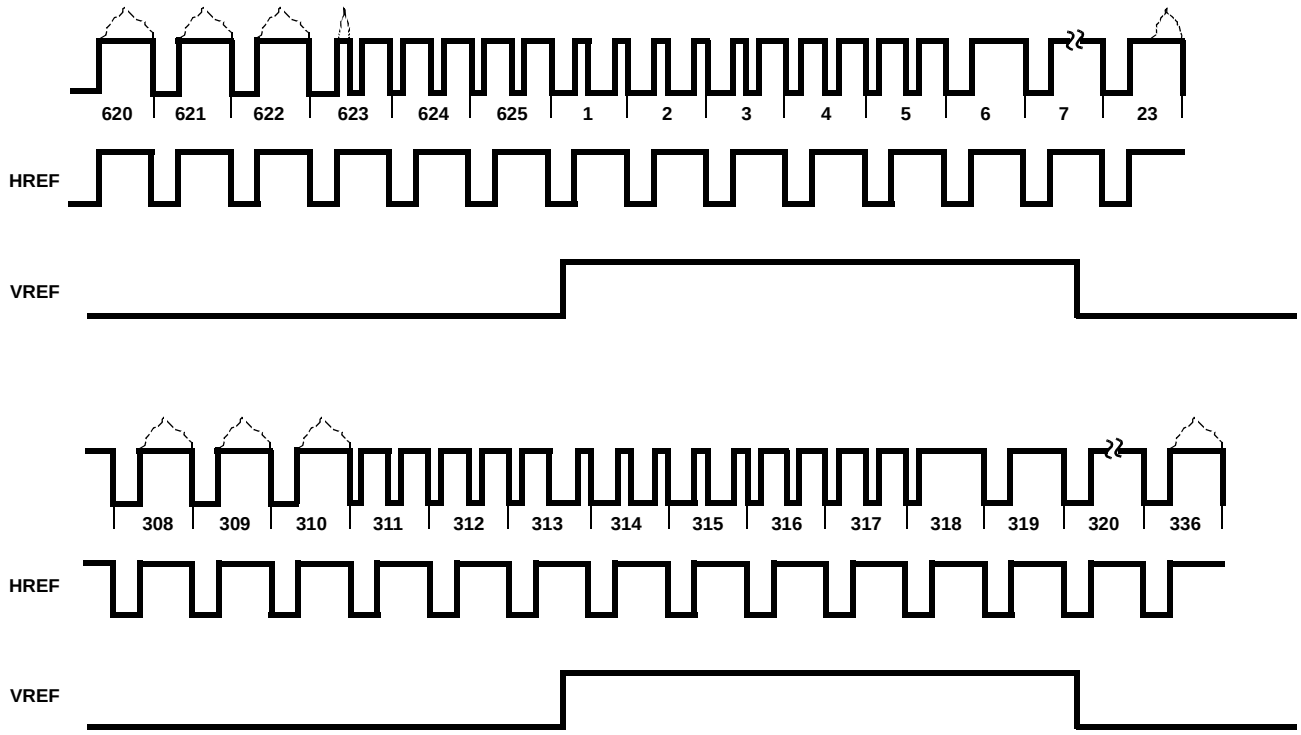


FIGURE 16. HREF AND VREF TIMING FOR 625/50 VIDEO SYSTEMS

Data Limits

YCbCr and blanking data should not use the 8-bit values of 00_H and FF_H since those values are used for timing information in BT.656 systems. For 10-bit systems, the 10-bit values 000_H–003_H and $3FC_H$–$3FF_H$ should not be used to avoid contention with 8-bit BT.656 systems.

During blanking intervals, Y values should be set to 10_H (040_H if a 10-bit system) and CbCr values set to 80_H (200_H if a 10-bit system).

Implementation Considerations

Video IC Receivers

Assumptions should not be made about the number of clock cycles per line or horizontal blanking interval. Otherwise, the implementation may not work with real-world video signal sources that use digital PLLs and proposed variations such as scaled video.

To ensure compatibility between various video sources, any horizontal counters should be reset by the leading edge of HREF, and not by the trailing edge of VACTIVE. Any vertical counters to count lines within a field should be reset by the leading edge of VREF.

Some video sources indicate sync timing by having Y data be a value of less than 16. However, most video ICs do not do this. In addition, to allow real-world video and test signals to be passed through with minimum disruption, many ICs now allow the Y data to have a value less than 16 during active video. Thus, receiver designs assuming sync timing will be present on the Y channel will no longer work.

To support video sources that do not generate a line-locked clock, the Data Valid signal (DVALID) is commonly supported. When both VACTIVE and DVALID are asserted, valid pixel data is present.

Video IC Sources

HREF and VREF have some unique output hold timings - thus, designers must be careful in designing VMI output interfaces. If these specifications are not met, there may be timing problems.

Summary

This Application Note presented some of the capabilities and issues of the Video Module Interface.

Video ICs that support VMI, such as the HMP8115 NTSC/PAL decoder, ease system design by simplifying video interfacing issues.